

REMARKS

This is intended as a full and complete response to the Office Action dated February 4, 2000, having a shortened statutory period for response set to expire on May 4, 2000. Claims 1-8, 11-18, 20, and 21 were considered and stand rejected. Applicants have amended the specification to remove informalities objected to by the Examiner and clarify the invention. Applicants assert no new matter has been introduced in this amendment.

Claims 1, 5, 15, 18, and 20 stand rejected under 35 U.S.C. §112, first paragraph. The Examiner asserts that replacement of "hole" with "feature" essentially adds new matter since the substituted "feature" has broader interpretation than hole, and "feature" was not described in the specification. Applicants respectfully traverse this rejection on grounds that "feature" and "hole" are terms of art in semi-conductor manufacturing whose meanings are understood by those with ordinary skill in the art. Further, the term feature as used in the claims is supported by the specification at page 6, lines 20-22, at page 7, lines 8-11, and at page 13, lines 8-16, by teaching that the invention encompasses the filling of features, such as a plug hole disclosed on page 5, lines 8-20. Withdrawal of the rejection of claims 1, 5, 15, 18, and 20 is respectfully requested.

Claims 1-6, 8, and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Taguchi et al.* in view of *Ho et al.*, and further in view of *Bunshah's Handbook of Deposition Technologies for Films and Coating* (hereinafter *Bunshah*). The Examiner asserts that it would have been obvious to one of ordinary skill in the art to fill the via-hole formed in a dielectric layer according to the method of *Taguchi et al.* as modified by the copper process of *Ho et al.* with the reactive sputtering method disclosed in *Bunshah*. Applicants respectfully traverse the rejection.

Taguchi et al. discloses a combination of barrier layers formed on the sidewalls of a hole in order to reduce titanium oxidation, thereby enhancing the reaction between titanium and aluminum to provide an improved wetting surface for an aluminum deposition. *Taguchi et al.* teaches conformal deposition of the second barrier layer within the feature and requires the formation of two barrier layers on the sidewalls of a hole. *Taguchi et al.* does not teach, show, or suggest removing a first barrier layer formed on the bottom of the feature and depositing a second barrier layer substantially on the bottom of the feature. Further, *Taguchi et al.* does not

teach, show, or suggest depositing a second barrier layer by a directional sputtering technique.

Ho et al. discloses the deposition of a conformal barrier seed layer over the bottom and sidewalls of an interconnect and then deposition of a conductive material on the conformal seed layer to fill the interconnect. *Ho et al.* does not teach, show, or suggest removing a first barrier layer formed on the bottom of the feature and depositing a second barrier layer substantially on the bottom of the feature. Further, *Ho et al.* does not teach, show, or suggest depositing a second barrier layer by a directional sputtering technique. Additionally, there is no suggestion or motivation in *Taguchi et al.* to modify the two barrier layer process for forming an improved titanium and aluminum wetting surface with the single barrier layer and copper deposition technique of *Ho et al.* to fill a feature in a dielectric layer as recited in the claims.

Bunshah discloses deposition of metal films by bias sputter deposition and does not teach, show, or suggest the use of a directional sputtering to deposit a metal layer, such as the second barrier layer as recited in claim 1. Thus, the Examiner fails to identify any suggestion or motivation in *Taguchi et al.* for modifying an improved titanium and aluminum wetting surface and deposition process by the barrier layer materials of the invention, for use with a copper deposition process of *Ho et al.*, or with the bias sputter deposition of *Bunshah* to teach the claimed invention. Therefore, *Taguchi et al.*, *Ho et al.*, and *Bunshah*, neither alone nor in combination, teach, show, or suggest depositing a first barrier layer on a bottom or sidewalls of a feature, removing the first barrier layer from the bottom of the feature, depositing a second barrier layer comprising Ta, TaN, TaSiN, TiSiN on substantially the bottom of the feature using a directional sputtering technique, and then depositing a metal layer in the feature. Withdrawal of the rejection to claims 1-6, 8, and 11 is respectfully requested.

Claims 7 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Taguchi et al.* in view of *Ho et al.* and *Bunshah*, and further in view of *Barnes et al.* The Examiner asserts that *Taguchi et al.* does not teach depositing a metal layer by PVD methods or by sputter deposition under conditions of a high density plasma, however, it would have been obvious to one of ordinary skill in the art to modify the CVD deposition technique of *Taguchi et al.* to sputter deposit the metal layer by high density physical vapor deposition techniques of *Barnes et al.* Applicants respectfully traverse the rejection.

Taguchi et al., *Ho et al.*, and *Bunshah* are distinguished above. *Barnes et al.* discloses an

apparatus for depositing material into high aspect ratio features by a high density plasma and does not teach, show, or suggest a method for filling a feature formed in a dielectric layer. *Barnes et al.* does not teach, show, or suggest depositing a second barrier layer on substantially the bottom of the feature using a directional sputtering technique. Therefore, *Barnes et al.* does not add to the combination of *Taguchi et al.*, *Ho et al.*, and *Bunshah*, to teach, show, or suggest removing a first barrier layer formed on the bottom of the feature and depositing a second barrier layer on substantially the bottom of the feature using a directional sputtering technique, and then depositing a metal layer in the feature. Withdrawal of the rejection to claims 7 and 12 is respectfully requested.

Claims 13 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Taguchi et al.* in view of *Ho et al.*, *Bunshah*, and *Barnes et al.*, and further in view of *Kurino et al.*. The Examiner asserts that it would have been obvious to use the temperature and pressure deposition regimes of *Kurino et al.* to deposit the metal layer of the claimed invention. Applicants respectfully traverse the rejection.

Taguchi et al., *Ho et al.*, *Bunshah*, and *Barnes et al.*, are distinguished above. *Kurino et al.* discloses etching a hole in one or more dielectric layers, depositing a barrier layer on the exposed surfaces of the etched hole, and filling the hole by depositing a conductive metal on the barrier layer and using high temperature and high pressure to force the conductive material to fill the hole. *Kurino et al.* does not add to the combination of *Taguchi et al.*, *Ho et al.*, *Bunshah*, and *Barnes et al.* to teach, show, or suggest removing the first barrier layer formed on the bottom of the feature, depositing a second barrier layer on substantially the bottom of the feature using a directional sputtering technique, and then depositing a metal layer comprising copper on the second barrier layer. Further, *Taguchi et al.*, *Ho et al.*, *Bunshah*, *Barnes et al.*, and *Kurino et al.* are silent as to depositing the metal layer by an electroplating process. Therefore, *Taguchi et al.*, *Ho et al.*, *Bunshah*, *Barnes et al.*, and *Kurino et al.*, neither alone nor in combination, teach, show, or suggest the claimed invention. Withdrawal of the rejection of claims 13 and 14 is respectfully requested.

Claims 15-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Taguchi et al.* in view of *Tseng et al.*. The Examiner has stated that it would have been obvious to modify the titanium and aluminum deposition process of *Taguchi et al.* by the polysilicon plug formation

process of *Tseng et al.*, to deposit a first barrier layer over a blanket dielectric layer and then form a via hole through the barrier layer and the dielectric layer prior to deposition of a second barrier layer. Applicants respectfully traverse the rejection.

Taguchi et al. describes a combination of barrier layers formed on the sidewalls of a hole in order to reduce titanium oxidation, thereby enhancing the reaction between titanium and aluminum to provide for improved aluminum deposition. *Taguchi et al.* does not teach, show, or suggest forming a feature through a barrier layer formed on a dielectric layer and through the dielectric layer. *Taguchi et al.* does not teach, show, or suggest depositing a barrier layer on the bottom and sidewalls of the feature. Further, *Taguchi et al.* does not teach, show, or suggest removing the barrier layer formed at the bottom of the feature prior to depositing a metal layer.

Tseng et al. discloses the formation of a polysilicon plug by depositing a first barrier layer over a blanket dielectric layer, forming a feature through the barrier layer and the dielectric layer to expose an underlayer, depositing a polysilicon fill layer in the feature, and removing the barrier layer from the blanket dielectric layer prior to deposition of a metal layer. *Tseng et al.* does not teach, show, or suggest depositing a barrier layer on the bottom and sidewalls of the feature. Further, *Tseng et al.* does not teach, show, or suggest removing the barrier layer formed at the bottom of the feature prior to depositing a metal layer. Additionally, there is no suggestion or motivation in *Taguchi et al.* or *Tseng et al.* to form a feature through a barrier layer formed on a dielectric layer and through the dielectric layer, deposit a barrier layer on the bottom and sidewalls of the feature, and remove the barrier layer formed at the bottom of the feature prior to depositing a metal layer.

Additionally, *Taguchi et al.* discloses a process to improve an aluminum metallization process and *Tseng et al.* teaches an improved technique to form polysilicon contact plugs for active silicon device elements. The metal free polysilicon plug formation process of *Tseng et al.* does not address the same or similar problems in the art as disclosed in the aluminum metallization process of *Taguchi et al.* and, therefore, it would not have been obvious to modify *Tseng et al.* by *Taguchi et al.* to produce the claimed invention. Further, modifying the aluminum metallization process of *Taguchi et al.* by the non-metal polysilicon plug formation process of *Tseng et al.* would render *Taguchi et al.* unsatisfactory for its intended purpose of forming a low oxide titanium layer on the sidewalls of a feature, and thus, destroys the *Taguchi*

et al. reference. See, *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Therefore, the combination of *Taguchi et al.* and *Tseng et al.* does not teach, show, or suggest forming a feature through a barrier layer formed on a dielectric layer and through the dielectric layer, depositing a barrier layer on the bottom and sidewalls of the feature, or removing the barrier layer formed at the bottom of the feature prior to depositing a metal layer. Withdrawal of the rejection of claims 15-18 is respectfully requested.

Claim 20 stands rejected under 35 U.S.C. 103(a) as being unpatentable over *Taguchi et al.* in view of *Ho et al.* and *Bunshah*, and further in view of *Gardner* and *Barnes et al.* The Examiner states it would have been obvious to modify *Taguchi et al.* to deposit a wetting layer before depositing the metal layer by physical vapor deposition techniques. Applicants respectfully traverse the rejection.

Taguchi et al., *Ho et al.*, *Bunshah*, and *Barnes et al.*, are distinguished above. *Gardner* discloses depositing a wetting layer by CVD and then depositing a copper layer on the wetting layer. *Gardner* does not teach, show, or suggest depositing the metal layer by a chemical vapor deposition technique, and then depositing the metal layer by a physical vapor deposition technique to fill the feature. *Gardner* does not add to the combination of *Taguchi et al.*, *Ho et al.*, *Bunshah*, and *Barnes et al.* to teach, show, or suggest removing a first barrier layer formed on the bottom of the feature and depositing a second barrier layer on substantially the bottom of the feature using a directional sputtering technique, and then depositing a metal layer in the feature. Therefore, *Taguchi et al.*, *Ho et al.*, *Bunshah*, *Barnes et al.*, and *Gardner*, neither alone nor in combination, teach, show, or suggest the claimed invention. Withdrawal of the rejection of claim 20 is respectfully requested.

Claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Taguchi et al.* in view of *Tseng et al.*, and further in view of *Ho et al.* The Examiner states that it would have been obvious to modify the combination of *Taguchi et al.* and *Tseng et al.* by the copper deposition technique of *Ho et al.* Applicants respectfully traverse the rejection.

As argued above for claims 15-18, *Taguchi et al.* could not be modified by *Tseng et al.* to teach, show, or suggest the claimed invention render *Taguchi et al.* unsatisfactory for its intended purpose of forming a low oxide titanium layer on the sidewalls of a feature. Further, as argued above for claims 1-6, 8, and 11 there is no suggestion or motivation in *Taguchi et al.* to modify

the combination of barrier layers to improve titanium and aluminum interaction with the single barrier layer and copper deposition technique of *Ho et al.* Additionally, there is no suggestion or motivation in the *Tseng et al.* metal free polysilicon plug formation process to use the copper and tantalum metallization process of *Ho et al.* since such a modification of *Tseng et al.* would render *Tseng et al.* unsatisfactory for its intended purpose and destroy the reference. Therefore, *Taguchi et al.*, *Ho et al.*, and *Tseng et al.*, neither alone nor in combination, teach, show, or suggest the claimed invention. Withdrawal of the rejection of claim 21 is respectfully requested.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the method or process of the present invention. Having addressed all issues set out in the office action, applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

Respectfully submitted,



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